AMENDMENTS TO THE SPECIFICATION

Please amend Paragraph 0016 and 0022 of the Specification as set forth below:

[0016] With reference to FIG. 6, a reference voltage generator 30 in accordance with one embodiment of the present invention is shown for use in the hysteresis circuit (as depicted in FIGS. 3 and 7). For the embodiment, the reference voltage generator 30 generates two distinct reference voltage levels. The reference voltage generator 30 includes: a first originator circuit 32 which generates a first reference voltage Vh+; a second originator circuit 34 which generates a second reference voltage Vh-; and a selector circuit 36 which selects as an output reference voltage one of the first and second reference voltages based upon the input signal to the hysteresis circuit undertaking a high-to-low (H-L) signal transition or low-to-high (L-H) signal transition, respectively. This embodiment of the reference voltage generator 30 takes the place of the prior art ~~voltage~~ reference voltage generator 12 in FIG. 3, with the rest of the hysteresis circuit 10 remaining identical to that shown in FIG. 3. Hence, when referring to the hysteresis circuit, the already provided discussion of the hysteresis circuit 10 in FIG. 3 shall be referred to. As is described hereinafter, the hysteresis circuit with the generator 30 is also described in respect to FIG. 7.

[0022] The selector circuit 36 includes an output reference voltage node 42 having the output reference voltage V_{REF}, which is provided to the input of the sensing amplifier 14 (FIGS. 3 and 7). The selector circuit 36 includes a fourth p-channel device P4 and a fourth n-channel device N4. The fourth p-channel device P4 has its drain coupled to the output ~~voltage~~ reference voltage node 42 and its source coupled to the first reference voltage node 38. The fourth n-channel device N4 has a drain coupled to the output ~~voltage~~ reference voltage node 42 and its source coupled to the second reference voltage node 40. The two gates of the transistors P4 and N4 are coupled to the output of the sensing amplifier 14 shown in FIGS 3 and 7.